--3. An integrated circuit die comprising:

A. a rectangular semiconductor substrate having four sides;

B. functional circuitry formed on the semiconductor substrate;

C. plural functional bond pads formed peripherally on the substrate and connected to the functional circuitry, there being a certain number of bond pads along each side of the substrate and the number of bond pads along at least two opposite sides being unequal; and

D. at least one bypass bond pad formed peripherally on the substrate along a side so that the total number of functional bond pads and bypass bond pads on opposite sides are equal.

--4. The die of claim 3 in which the functional bond pads include inputs, outputs, voltage and ground.

--5. The die of claim 3 including a mode bond pad formed peripherally on the substrate along one side in addition to the total number of functional bond pads and bypass bond pads.

--6. An integrated circuit die comprising:

A. a rectangular semiconductor substrate having four sides;

B. functional circuitry formed on the semiconductor substrate;

C. plural bond pads formed peripherally on the substrate and connected to the functional circuitry, there being a certain number of bond pads along each side of the substrate and the number of bond pads along at least two opposite sides being equal;

D. plural conductors formed on the substrate and selectably connecting each bond pad on one side of the substrate with a corresponding bond pad on the opposite side of the substrate.

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--7. The die of claim 6 including switching circuits formed on the substrate and selectably connecting each conductor to a bond pad and its corresponding bond pad on the opposite side of the substrate.

--8. The die of claim 6 including switching circuits formed on the substrate and selectably connecting each conductor to a ground potential.

--9. The die of claim 6 including switching circuits formed on the substrate and selectably connecting each conductor to a bond pad and its corresponding bond pad on the opposite side of the

substrate and including a mode ~~bond pad connected to the switching circuits.~~

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--10. An integrated circuit comprising:

A. functional circuitry having functional input leads and functional output leads;

B. at least one conductor separate from the functional circuitry, the functional input leads and the functional output leads;

C. a first switching circuit having a first lead connected to one of the functional input leads and functional output leads, a second lead connected to the at least one conductor, and a third control lead;

D. a second switching circuit having a first lead connected to another one of the functional input leads and functional output leads, a second lead connected to the at least one conductor, and a third control lead; and

E. a control signal lead connected to the third control lead of the first and second switching circuits.

--11. The integrated circuit of claim 10 in which the first and second switching circuits each include a fourth lead connected to a ground potential.

--12. The integrated circuit of claim 10 in which the first switching circuit connects to a functional input lead and including a third switching circuit connected in series in the functional input lead between the first switching circuit and the functional circuitry.

--13. A process of bypassing functional circuitry on an integrated circuit comprising:

A. receiving a mode control signal at the integrated circuit;

B. forming conducting paths between selected ones of functional circuitry input leads and output leads in response to receiving the mode control signal;

C. passing signals through the conducting paths.

--14. The process of claim 13 in which the forming includes forming conducting paths that are separate from the functional circuitry.

--15. The process of claim 13 in which the forming includes forming conductive paths from a bond pad on one side of the integrated circuit to a corresponding bond pad on an opposite side of the integrated circuit.

--16. An integrated circuit comprising:

A. functional circuitry having input and output leads;

B. a ground lead carrying a reference potential;

C. plural conductors separate from the functional circuitry; and

D. switching circuits selectably connecting the conductors between the input and output leads and the ground lead.

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--17. A wafer of semiconductor material comprising:

A. plural dies formed on the wafer, each die including functional circuitry and bond pads, each die having a voltage bond pad receiving a supply voltage and having a ground bond pad receiving a supply ground;

B. a first probe area formed on the wafer separate from the dies;

C. a first array of conductors connecting the first probe area to the voltage bond pad of all the dies; and

D. a second probe area formed on the wafer separate from the dies;

E. a second array of conductors connecting the first probe area to the ground bond pad of all the dies.

--18. The wafer of claim 17 in which there are two first probe areas and two second probe areas.

--19. The wafer of claim 17 including a forward biased diode between the first array of conductors and each die and a forward biased diode between each die and the second array of conductors.

--20. An electronic system comprising:

~~A.~~ a first circuit having a mode input lead receiving a mode signal to place the first circuit in one of a first and second mode; and

~~B.~~ a second circuit having a mode output lead connected to the mode input lead of the first circuit and having first and second clock leads separate from the first circuit, at least one of the clock leads receiving a clock signal that controls a mode signal formed on the mode output lead.

--21. The system of claim 20 in which the first circuit includes functional circuitry, the first mode is a functional mode and the second mode is a by-pass mode.

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--22. The system of claim 20 in which the second circuit is a die selector circuit that includes D-type flip-flops, AND gates, OR gates and delay elements.

--23. The system of claim 20 in which the first and second clock leads are both capable of receiving and sending clock signals.

--24. The system of claim 20 in which the second circuit includes clock input and output buffers and a state machine.

--25. The system of claim 20 in which the second circuit includes third and fourth clock leads separate from the first circuit and at least one of the four clock leads receives a clock signal that controls the mode signal.

--26. The system of claim 20 in which the second circuit includes third and fourth clock leads separate from the first circuit, clock input buffers, clock output buffers and a state machine.

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--27. An electronic circuit comprising:

A. a first clock lead connected to first input and output buffers;

B. a second clock lead connected to second input and output buffers;

C. a mode lead connected to a mode output device; and

D. a state machine connected to the first and second input and output buffers and connected to the mode output device.

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--28. The circuit of claim 27 including a first connection from the first input buffer to the second output buffer and a second connection from the second input buffer to the first output buffer.

--29. The circuit of claim 27 in which the state machine has inputs connected to the outputs of the first and second input buffers and has outputs connected to control the first and second output buffers.

--30. A process of operating a circuit comprising:

A. producing a mode output signal of one state;

B. receiving a first clock signal having a leading rising and a trailing falling edge on one lead;

C. producing a mode output signal of another state in response to the falling edge of the first clock signal;

D. receiving a second clock signal having a leading rising edge and a trailing falling edge;

E. outputting the second clock signal in response to the falling edge of the first clock signal; and

A2 F. producing a mode signal of the first state in response to the rising edge of the second clock signal.

--31. The process of claim 30 in which the outputting the second clock signal includes connecting a first lead, which receives the first and second clock signals, to a second lead in response to the falling edge of the first clock signal and outputting the second clock signal on the second lead.

--32. The process of claim 30 including receiving subsequent clock signals and outputting the subsequent clock signals while maintaining the state of the mode signal.

--33. The process of claim 30 in which the ~~first state of~~ the mode signal is a ~~by-pass mode~~ and the second state of the mode ~~signal is~~ a functional mode.

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--34. A process of selecting sequential ones of a series of plural functional circuits comprising:

A. placing all of the functional circuits in an unselected mode;

B. using a first clock signal applied to one lead to place a first functional circuit in a selected mode while maintaining the remaining functional circuits in the unselected mode;

A2 Cont. C. using a second clock signal applied to the lead to return the first functional circuit to the unselected mode and to place a second functional circuit in the series in the selected mode while maintaining the remaining functional circuits in the unselected mode; and

D. using a third clock signal applied to the lead to return the second functional circuit to the unselected mode and to place a third functional circuit in the series in the selected mode while maintaining the remaining functional circuits in the unselected mode.